MC-XIL-UART Asynchronous Communications Core

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Features

- Supports Spartan™-3, Virtex™-II, and Virtex-II Pro™ FPGAs
- Function compatible with Industry Standard 8250 UART with external microprocessor interface.
- Combined UART and Baud Rate Generator
- DC to 3.75 Mbps (DC to 60 MHz Clock)
- 1 to 65535 divisor generates 16X clock enable
- Prioritized interrupt mode
- Modem interface
- Line break generation and detection
- Loopback mode
- Available under terms of the SignOnce IP License

AllianceCORE™ Facts

Core Specifics	
See Table 1	
Provided with Core	
Documentation	User Guide
Design File Formats	Verilog or VHDL source files[1]
Verification	Machine-readable simulation vectors for Verilog or VHDL
Constraints File	.ucf
Instantiation Templates	VHDL, Verilog
Reference designs & application notes	None
Additional Items	Warranty by MemecCore
Simulator Tool Used	
ModelSim 5.5d	
Support	
Core support provided by MemecCore Additional customization provided by Memec Design	

Notes:
1. Synplify Pro 7.2 used for synthesis of netlists.

Applications

- Serial data communications applications
- Logic consolidation

Table 1: Core Implementation Data

Supported Family	Example Device[1]	Fmax (MHz)[2]	Slices	IOB[3]	GCLK	BRAM	MULT	DCM/ DLL	MGT	PPC	Design Tools
Spartan-3	XC3S50-4	99	144	94	1	0	0	0	N/A	N/A	ISE 5.1i
Virtex-II	XC2V80-6	183	144	94	1	0	0	0	N/A	N/A	ISE 5.1i
Virtex-II Pro	XC2VP2-7	228	144	94	1	0	0	0	0	0	ISE 5.1i

Notes:
1. Specific devices are minimum size and speed recommended.
2. Optimized for speed.
3. Assuming all core signals are routed off-chip.

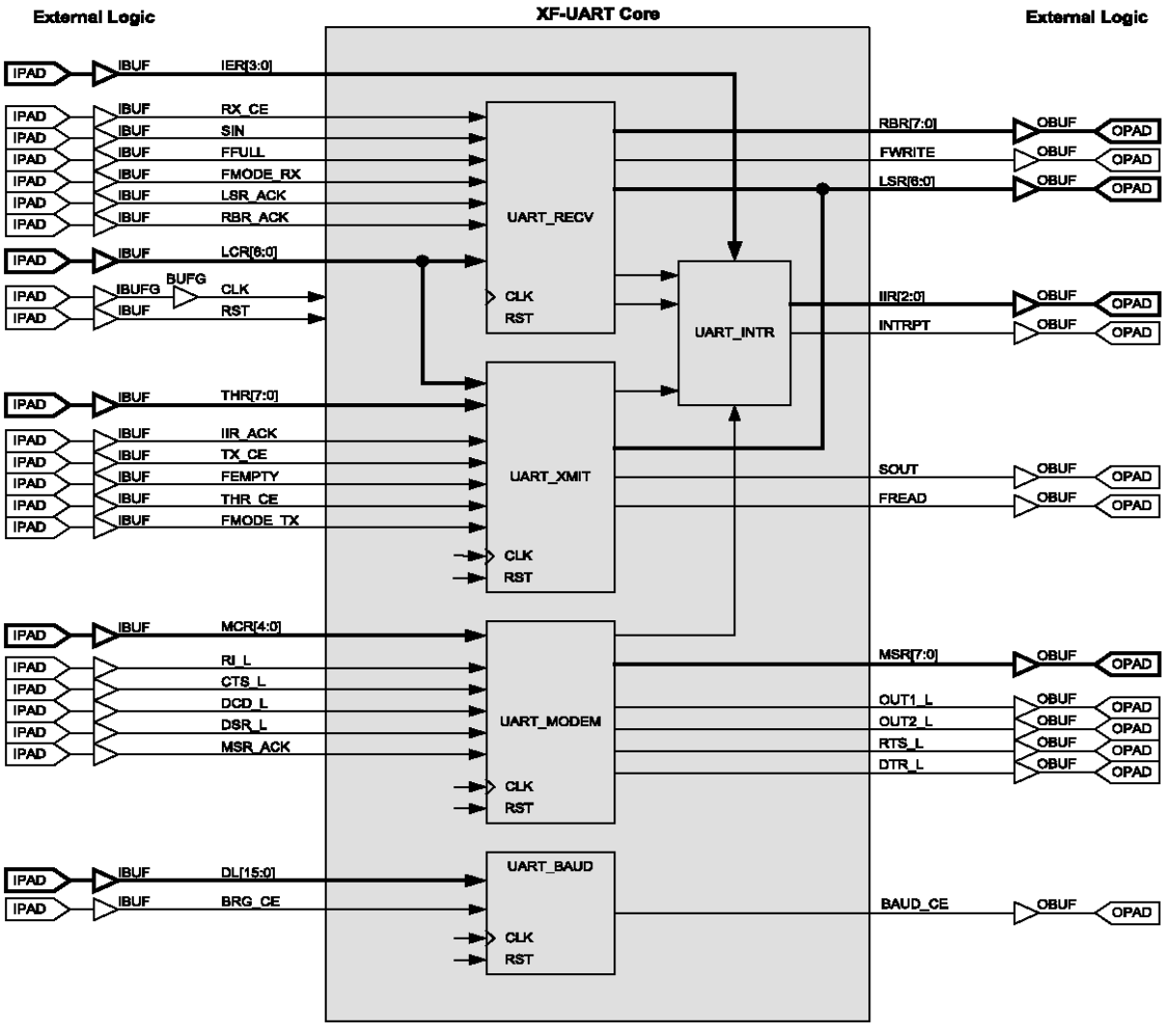

Figure 1: MC-UART Block Diagram

General Description

The MC-XIL-UART Asynchronous Communications Core is a high-performance programmable Universal Asynchronous Receiver/Transmitter (UART) and Baud Rate Generator (BRG).

The microprocessor interface is outside of the core. This allows greater flexibility in interfacing to the user's logic. The microprocessor interface is supplied as a reference design.

The MC-XIL-UART is a tailored replacement of our popular MC8250 Asynchronous Communications Core optimized for Xilinx FPGAs.

Functional Description

The MC-XIL-UART CORE along with external pads is shown in block diagram in Figure 1.

The MC-XIL-UART is partitioned into modules. These modules are described below.

UART_RECV: Receiver

This block filters the serial input data (SIN), detects the start bit, controls the sampling of SIN, determines when a complete character is shifted into the receive shift register, and stores the received character into the Receive Buffer Register (RBR) or an external FIFO. The RBR can be bypassed if an external FIFO is used. Parity, framing, and overrun errors are detected and their corresponding bits are set in the line status register (LSR). This block also

generates interrupts for receive data available and the receiver's error status. All operations in this block are synchronous to CLK and enabled with the receiver clock enable, RX_CE. RX_CE must occur at 16x the expected serial bit rate.

UART_XMIT: Transmitter

This block accepts 8-bit parallel data, serializes it, appends start, stop, and parity bits as needed, and shifts this data out on SOUT. A Transmitter Holding Register (THR) is used to "double buffer" the input data for increased throughput. The THR can be bypassed if an external FIFO is used. This block generates an interrupt when the THR or external FIFO is empty. All operations in this block are synchronous to CLK and enabled with the transmitter clock enable, TX_CE, except writing data to the THR which is synchronous to CLK and enabled with the THR_CE. TX_CE must occur at 16x the desired serial bit rate.

UART_MODEM: Modem Control and Status Logic

This block provides status of the modem input lines, both current status and change of state. The modem control lines are also generated here. An interrupt is generated on the low to high transition of RI_L or any change of state of CTS_L, DCD_L, and DSR_L. All operations in this block are synchronous to CLK.

UART_BAUD: Baud Rate Generator

This block provides a divide by n of the CLK input, where n is the 16-bit input value presented on DL[15:0]. Any change on DL[15:0] is detected and immediately loaded into the internal counter. The output, BAUD_CE, is typically set to 16x the serial bit rate. If a 16-bit divisor is not sufficient, an external prescaler can drive the BRG_CE input. All operations in this block are synchronous to CLK and enabled with the clock enable, BRG_CE.

UART_INTR: Interrupt Logic

This block prioritizes the four interrupt sources and encodes them into a 3-bit Interrupt Identification Register value, IIR[2:0], and generates the interrupt request output, INTRPT. A 4-bit Interrupt Enable Register input, IER[3:0], allows the user to individually mask each interrupt input. Any active interrupt source that has its corresponding IER bit set will cause INTRPT to be asserted.

Core Assumptions

In order to use this core in a standard 8250-type application, external microprocessor interface logic must be added. Refer to the User's Guide.

The main differences between MC-XIL-UART and 8250 are as follows:

- The MC-XIL-UART cannot drop into all industry standard 8250 applications because it does not have a separate receiver clock input and because the baud rate generator output is a single clock pulse wide.
- The MC-XIL-UART is synchronous to one clock input, whereas the standard core has three clock buffers for the UART logic and another for the microprocessor write strobe.
- The MC-XIL-UART has some signals brought out to facilitate interfacing to transmit and receive FIFOs.
- MC-XIL-UART does not support 1½ stop bits.

Core Modifications

Customizing is available through MemecCore.

Verification Methods

Complete functional and timing simulation has been performed on the MC-XIL-UART using a Verilog Simulator (simulation vectors used for verification are provided with the core). This core has also been used successfully in customer designs.

Recommended Design Experience

Users should be familiar with Verilog. Users should also have experience with microprocessor systems and asynchronous communication controllers.

Available Support Products

MemecCore provides MC-XIL-UART Asynchronous Communications Core.

Pinout

The pinout of the MC-XIL-UART core has not been fixed to specific FPGA I/O, allowing flexibility with a user's application. Signal names are shown in Figure 1 and described in Table 2.

Table 2: Core Signal Pinout

Signal Name	Signal Direction	Description
SIN	Input	Serial Data In.
SOUT	Output	Serial Data Out.
TX_CE	Input	Transmitter Clock Enable.
RX_CE	Input	Receiver Clock Enable.
BAUD_CE	Output	Baud Rate Generator Out.
CTS_L	Input	Clear To Send (active low).
DSR_L	Input	Data Set Ready (active low).
DCD_L	Input	Data Carrier Detect (active low).
RI_L	Input	Ring Indicator (active low).
RTS_L	Output	Request To Send (active low).
DTR_L	Output	Data Terminal Ready (active low).
OUT1_L	Output	Output 1 (active low).
OUT2_L	Output	Output 2 (active low).
DL[15:0]	Input	Divisor Latch.
LCR[6:0]	Input	Line Control Register.
MCR[4:0]	Input	Modem Control Register.
IER[3:0]	Input	Interrupt Enable Register.
FMODE_TX	Input	Transmitter FIFO Mode Select
THR[7:0]	Input	Transmitter Holding Register Data In.
THR_CE	Input	Transmitter Holding Register Clock Enable.
FREAD	Output	FIFO Read.
FEMPTY	Input	FIFO Empty Flag.
FMODE_RX	Input	Receiver FIFO Mode Select.
RBR[7:0]	Output	Receiver Buffer Register.
FWRITE	Output	FIFO Write Enable.
FFULL	Input	FIFO Full Flag.
RBR_ACK	Input	Receiver Buffer Register Read Acknowledge.
IIR_ACK	Input	Interrupt Identification Register Read Acknowledge.
LSR_ACK	Input	Line Status Register Read Acknowledge.
MSR_ACK	Input	Modem Status Register Read Acknowledge.
LSR[6:0]	Output	Line Status Register.
MSR[7:0]	Output	Modem Status Register.
IIR[2:0]	Output	Interrupt Identification Register.
INTRPT	Output	Interrupt Request.
CLK	Input	System Clock Input.
RST	Input	System Reset.
BRG_CE	Input	Baud Rate Generator Clock Enable.

Ordering Information

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For AllianceCORE specific information:

URL: www.xilinx.com/products/logicore/alliance/tblpart.htm